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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte YUTAKA HAGA

Appeal 2008-006001
Application 09/778,076
Technology Center 2100

Before JAMES D. THOMAS, HOWARD B. BLANKENSHIP, and JEAN R. HOMERE, *Administrative Patent Judges*.

THOMAS, *Administrative Patent Judge.*

DECISION ON APPEAL[1]

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's twice rejection of claims 8 through 17, 19 through 28, and 30 through 42. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Invention

According to an apparatus for collecting a profile of a program, a CPU generates an interrupt when a branch instruction is executed during the execution of the program. In this interrupt, an analyzing section determines whether the executed branch instruction is an instruction relating to the execution of a subroutine, and, in the case where the branch instruction is an instruction relating to the execution of the subroutine, a collecting section extracts a profile of the subroutine and stores it in a profile memory section. (Spec. 45, Abstract; Figs. 2B, 3A-B.)

Representative Claim

12. An apparatus for collecting a profile of a subroutine included in a program, comprising:

a storage unit storing a profile;

an analyzing section, when an interrupt is generated by execution of a branch instruction during execution of said program:

obtaining a branch source address and a branch destination address from a source of said interrupt, and

identifying a type of said branch instruction by obtaining an instruction code from said branch source address and decoding said instruction code; and

a collecting section:

obtaining said branch source address, said branch destination address, and an identified result from said analyzing section when the identified instruction is a calling instruction or a return instruction of said subroutine; and

when said identified result is said calling instruction, storing said branch destination address as a subroutine address corresponding to said calling instruction and a calling time of said subroutine corresponding to said calling instruction in said storage unit,

when said identified result is said return instruction,

obtaining a return time of said subroutine corresponding to said return instruction,

calculating a execution time of said subroutine based on said obtained return time and said calling time, and

storing a cumulative value of said execution time as said profile in correspondence with said branch destination address in said storage unit, and

when the identified branch instruction is neither a calling instruction nor a return instruction, said interrupt is terminated.

Prior Art and Examiner's Rejection

The Examiner relies on the following references as evidence of unpatentability:

Alexander	6,002,872	Dec. 14, 1999
Smolders	6,253,338 B1	Jun. 26, 2001 (filed Dec. 21, 1998)
Yeh	6,427,206 B1	Jul. 30, 2002 (filed May 3, 1999)

All claims on appeal, claims 8 through 17, 19 through 28, and 30 through 42, stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the Examiner relies upon Alexander in view of Smolders, further in view of Yeh.

Claim Groupings

Based upon Appellant's arguments in the principal Brief on appeal, Appellant argues only independent claim 12 as representative of the subject matter of independent claims 12, 23, and 34. Separate arguments are presented as to dependent claim 40. Appellant refers to certain other claims by merely indicating what they "recite" and therefore relies for patentability upon the subject matter of representative independent claim 12 on appeal.

ANALYSIS

We refer to, rely on, and adopt the Examiner's findings and conclusions with respect to the applied prior art as well as the Examiner's responsive arguments to the positions set forth by Appellant in the principal

Brief on appeal. Our discussion will be limited to the followings points of emphasis.

To the extent Appellant takes a broad a position that the applied prior art is not properly combinable within 35 U.S.C. § 103, all three references generally relate to the concept of interrupt processing and two references specifically relate to monitoring of this processing within a computer. We agree with the Examiner's view that Smolders supplements the profiling system of Alexander. Not only does Alexander teach using a time-based interrupt as a basis for his structured profiling of computers, Alexander also teaches two other types of interrupts. While on the one hand the majority of the teachings in Alexander are concerned with an initial embodiment relating to sampling instruction sequencing, a second embodiment, which is discussed beginning at column 8, line 41, indicates that his monitoring processes may be applied to memory analysis and, in particular, page fault interrupts that are used to signal the monitoring system of Alexander to gather data from a stack memory. As the Examiner also noted, column 11, lines 23 through 25 further explicitly teach that other interrupts may be used to trigger the described sampling mechanism disclosed.

On this basis, it would have been fairly straight forward for a person of ordinary skill in the art to have supplemented/extended the teachings of Alexander with his use of a trace interrupt after each branch instruction as the title of Smolders reveals. Although we acknowledge that Yeh may be less pertinent to the monitoring of processes within a computer than Alexander and Smolders are, we recognize that Yeh indicates that various "types" of branch instructions may be characterized, such as, a call, a return,

and a regular branch. The discussion at column 1 of Yeh teaches the conventional understanding in the art of unconditional and conditional branching concepts to begin with.

Thus, from an artisan's perspective, "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 416 (2007).

Appellant's disclosed and claimed invention is based upon the well-known Intel brand of microprocessors in the art as discussed at pages 7 through 9 of the Specification that permit a processor to record a source and destination address of a branch instruction. On the other hand, Alexander specifically refers to the Intel brand of microprocessors at column 5 in a substantially corresponding manner. Additionally, other known prior art processing systems that process interrupts are identified in Yeh as taught at the bottom of column 2 with respect figure 1 of that reference.

Appellant's initial argument at page 12 of the principal Brief that Alexander fails to identify a type of branch instruction by obtaining instruction code as well as the branch source address and decoding address is misplaced. Although we have recognized that Alexander does not explicitly teach his invention as applicable to branch instructions per se, together with Smolders, this teaching is known in the art. Figure 2 of Alexander relates to a call stack which stores call or branch type addresses and return addresses. Thus, the artisan may consider Alexander as teaching branch instruction processing in other words. As noted by the Examiner, figure 4A illustrates a trace or profile of such call and return addresses and

instructions and figure 3 specifically illustrates a call stack sample to include identifying data for a process and for a thread of it as well as call and return addresses. Figure 5 illustrates in a different form a call stack tree that identifies these addresses, the base time and cumulative times as well as pertinent parent and child pointers, which the art regards as a form of address. Figure 6 illustrates the process under which the call stack is created and figure 7 illustrates a process to in turn identify the specific process or function involved within the computer. Subsequent figures identify the second embodiment relating to memory address profiling as well as different manners of presenting or recording the sample data as well as illustrating the nature of the data that is sampled.

In like manner, we also do not agree with Appellant's position at page 12 of the principal Brief that the applied prior art does not teach that an interrupt is terminated when it is determined that it is neither a calling instruction nor a return instruction. Alexander appears to illustrate this feature with the decision block 610 in figure 6 and the corresponding decision block 1104 in figure 11. With respect to the figure 2 showing in Smolders, the discussion at the bottom half of column 3 indicates the ability to specifically disable monitoring on an ad hoc or discretionary basis.

Appellant's additional argument at page 14 of the principal Brief relating to the claimed return address has been addressed earlier in this Opinion with respect to the noted teachings in Alexander. It is clear to a person of ordinary skill in the art in figure 3 of Smolders that particular addresses regarding trace interrupts for branch instructions are also placed in a trace buffer and are therefore profiled.

Lastly, we turn to the subject matter of dependent claim 40. We are persuaded by the Examiner's initial statement of the rejection beginning at page 11 of the Answer as well as the Examiner's responsive arguments as to this claim beginning at the bottom of page 16 of the Answer. We have set forth earlier some exemplary types of data or data structures that may be characterized as being monitored, recorded or otherwise profiled with respect to interrupt processing of instructions as well as memory addresses within the computer arts. In this regard, both Alexander and Smolders teach extensively utilizing different names and characterizations of data that are collected for monitoring purposes. We are equally persuaded by the Examiner's reasoning, principally at page 17 of the Answer, that the nature of the data characterized within the data structures identified in claim 40 is considered arbitrary and without any functional distinctions associated with it. Moreover, the use of the infinitive "to assign" within claim 40 in at least two locations of it does not recite a present tense functionality associated with the data structures identified. As such, the claim appears to be an attempt to seek patent protection for arbitrarily labeled data.

CONCLUSION AND DECISION

Appellant has not shown that the Examiner erred in finding that Alexander and Smolders, further in view of Yeh, teach the subject matter of the argued claims on appeal rejected within 35 U.S.C. § 103. Therefore, the Examiner's rejection on this statutory basis of all claims on appeal, claims 8 through 17, 19 through 28, and 30 through 42, is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

msc

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